Appl. No. 10/708,648
Amdt. Dated 05/03/2006
Reply to Office action of March 3, 2006

Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently Amended) A method of forming an oxidized tantalum nitride hardmask for dual damascene processing, comprising:

providing a semiconductor wafer, said wafer comprising:

a base dielectric layer;

a cap layer overlying the base dielectric layer;

a dielectric layer overlying the cap layer;

one or more hardmask layers overlying the dielectric layer; and

a tantalum nitride top hardmask layer having a thickness of 5-25nm overlying the one or more hardmask layers;

subjecting the tantalum nitride top hardmask layer to an oxidation process to convert said tantalum nitride top hardmask layer to an oxidized tantalum nitride (TaOxNx) top hardmask layer having a thickness of 2-4 times thicker and an increased transparency by a factor of more than 10 times than that of the tantalum nitride top hardmask layer.

2. (Original) A method according to claim 1, wherein the base dielectric layer includes planarized circuit elements to which an electrical connection is to be made.

3. (Original) A method according to claim 1, wherein the dielectric layer is a single dielectric.

4. (Original) A method according to claim 1, wherein the dielectric layer is a hybrid dielectric.

5. (previously presented) A method according to claim 6, wherein the oxidation process

further comprises:

providing an oxidation environment with a N20 flow rate between 500 and 5000 sccm at a chamber pressure between 1 and 10 Torr;

providing a wafer substrate temperature between 250 degrees C and 400 degrees C; and

providing a plasma power between 250 Watts and 1000 Watts.

6. (Original) A method according to claim 1, wherein the oxidation process is a combined thermal and plasma oxidation process.

7. (Original) A method according to claim 1, further comprising creating a patterned photoresist layer and etching the tantalum nitride layer prior to oxidation.

8. (Original) A method according to claim 1, further comprising creating a patterned photoresist layer and etching the oxidized tantalum nitride layer after the oxidation process.

9. (Currently Amended) A dual damascene method of processing a semiconductor wafer, comprising:

providing a semiconductor wafer having a base dielectric layer, said base dielectric layer having circuit elements embedded therein and planarized flush with the surface thereof to which a subsequent electrical connection is to be made;

forming a cap layer over the base dielectric layer and circuit elements;

forming a dielectric layer over the cap layer;

forming a first hardmask layer (HM1) over the dielectric layer;

forming a second hardmask layer (HM2) over the first hardmask layer;

forming a tantalum nitride top hardmask layer having a thickness of 5-25nm over the second hardmask layer;

lithographically etching the tantalum nitride top hardmask layer to form trench openings therein; and

subjecting the etched tantalum nitride top hardmask layer to an oxidation process to ~~form an~~ convert the tantalum nitride top hardmask layer to an oxidized tantalum nitride top hardmask layer having a thickness of 2-4 times thicker than the tantalum nitride top hardmask layer.

10. (Original) A method according to claim 9, wherein the dielectric layer is a single dielectric layer.

11. (Original) A method according to claim 9, wherein the dielectric layer is a hybrid dielectric layer.

12. (previously presented) A method according to claim 9, wherein the oxidation process is a thermal and plasma oxidation process.

13. (previously presented) A method according to claim 12, wherein the oxidation process further comprises:

providing an oxidation environment with a N20 flow rate between 500 and 5000 sccm at a chamber pressure between 1 and 10 Torr;

providing a wafer substrate temperature between 250 degrees C and 400 degrees C; and

providing a plasma power between 250 Watts and 1000 Watts.

14. (Currently Amended) A dual-damascene method of processing a semiconductor wafer, comprising:

providing a semiconductor wafer having a base dielectric layer, said base dielectric layer having circuit elements embedded therein and planarized flush with the surface thereof to which a subsequent electrical connection is to be made;

forming a cap layer over the base dielectric layer and circuit elements;

forming a dielectric layer over the cap layer;

forming a first hardmask layer (HM1) over the dielectric layer;

forming a second hardmask layer (HM2) over the first hardmask layer;

forming a tantalum nitride top hardmask layer having a thickness of 5-25nm over the second hardmask layer;

subjecting the tantalum nitride layer to an oxidation process to form an oxidized tantalum nitride top hardmask layer having a thickness of 2-4 times thicker than the tantalum nitride top hardmask layer; and

lithographically etching the oxidized tantalum nitride top hardmask layer to form trench openings therein.

15. (Original) A method according to claim 14, wherein the dielectric layer is a single dielectric layer.

16. (Original) A method according to claim 14, wherein the dielectric layer is a hybrid dielectric layer.

17. (Original) A method according to claim 14, wherein the oxidation process is a thermal and plasma oxidation process.

18. (Original) A method according to claim 17, wherein the oxidation process comprises:

providing an oxidation environment with a N20 flow rate between 500 and 5000 sccm at a chamber pressure between 1 and 10 Torr;

providing a wafer substrate temperature between 250 degrees C and 400 degrees C; and

providing a plasma power between 250 Watts and 1000 Watts.